REMARKS/ARGUMENTS

Claims 1, 3, 8 and 12-14 stand rejected, with claims 4-7 and 9-11 objected to in the outstanding Official Action. Claim 1 has been amended and therefore claims 1-14 remain in this application.

The Examiner's approval or objection to the originally filed formal drawings is normally noted on the Office Action Summary Sheet. Clarification as to whether the originally filed formal drawings are accepted by the Patent Office is respectfully requested.

The Examiner's consideration of the prior art submitted in Applicants' previously submitted Information Disclosure Statement is very much appreciated.

Claims 1, 3, 8 and 12-14 stand rejected under 35 USC §103 as being unpatentable over Trivedi (U.S. Patent 6,430,674). The Examiner suggests that Trivedi not only teaches all claimed elements in Applicants' rejected claims, but that it would be obvious to combine those elements in the claimed manner in view of the single Trivedi reference. Applicants have made minor modifications in claim 1 to more positively recite the structures and interrelationship between structures which are believed to comprise Applicants' invention.

Thus, Applicants' data processing apparatus requires a "processor core," a "prefetch unit" and a "prediction logic," where the prediction logic accomplishes a number of tasks, i.e., "predicting which instruction should be prefetched by the prefetch unit," "reviewing a prefetched instruction to predict whether execution of that prefetched instruction will cause a change in instruction flow," "indicating to the prefetch unit an address within said memory from which a next instruction should be retrieved," "predicting whether the prefetched instruction will additionally cause a change in instruction set" and "causing an instruction set identification

signal to be generated for sending to the processor core to indicate the instruction set to which said next instruction belongs."

It is noted that in order for Trivedi to render obvious Applicants' claimed combination of elements, each of the above structures must be disclosed or obvious in view of Trivedi, and in addition, there must be some disclosure or suggestion for interrelating these structures as set out in Applicants' claim. It is Applicants' position that not only are the recited structures not present in the Trivedi reference, there is also no suggestion or reason for combining the structures in the manner of Applicants' independent claim 1. As a result, Applicants are of the belief that the Patent Office has failed to set out a *prima facie* case of obviousness of independent claim 1 or any claims dependent thereon.

Examining the Official Action, the Examiner admits on page 3, section 4, that "Trivedi did not expressly detail (claim 1,13,14) a prefetch unit for prefetching instructions prior to sending those to the processor core." Applicants take this admission to be a confirmation that the Trivedi reference does not teach applicants' claimed "prefetch unit." Should Applicants have misinterpreted the Examiner's statement, clarification as to where and how the Examiner believes Trivedi to teach Applicants' claimed prefetch unit is respectfully requested.

Assuming the prefetch not to be disclosed in the Trivedi reference (as admitted by the Examiner), there is no indication of any prior art reference which does teach such a structure. Additionally, applicants find it impossible to find any disclosure in the Trivedi reference which teaches Applicants' claimed prediction logic for predicting which instructions "should be prefetched by the prefetch unit." Clearly, if there is no prefetch unit, it would seem strange that Trivedi would teach a prediction logic for predicting which instructions should be prefetched by the nonexistent prefetch unit.

Therefore, it would appear that, based upon the single admission by the Examiner on page 3, section 4, not only is the prefetch unit missing from the Trivedi reference, but also Applicants' claimed "prediction logic" would appear to necessarily absent as well. While processor cores are old, the Examiner appears to have admitted that the other recited structures in Applicants' claim 1 are missing from the Trivedi reference. Should this be the case, there is clearly no *prima facie* basis for rejecting claim 1, at least upon the Trivedi reference.

Examining the Trivedi reference somewhat more closely, and the Examiner's arguments concerning the Trivedi reference, Trivedi merely discloses a processor that can execute instructions from two different instruction sets. When Trivedi's processor needs to change its mode of operation, a detector 306 is provided to detect the presence of mode switch instructions in the decoder and generate a speculative wake-up signal upon such detection (Trivedi column 4, lines 24-27). This "wake-up" signal is routed to translator 302c (shown in Figure 3), which then outputs prestored transition instructions 502 (as in Figure 6) to the decoder, causing those transition instructions to then be executed within execution unit 304 to produce a transition in the mode of operation of the processor (see Trivedi column 6, line 29 to column 7, line 50). The whole point of the Trivedi elements and their interrelationship is to reduce the delay in transitioning between different instruction sets (Trivedi column 2, lines 35-36).

While the Examiner makes general reference to the Trivedi patent at column 3, lines 34-62, column 6, line 29 to column 7, line 50 and column 8, lines 35-58, as disclosing features of Applicants' claim 1, it is submitted that none of the cited portions of Trivedi contain any such teaching. When examined in detail, Trivedi at column 3, lines 35-62 merely describes the fact that the processor can execute instructions from both first and second instruction sets. The text between column 6, line 29 through column 7, line 50 describes the use of the detector 306 to

detect the presence of a mode switch instruction and to cause a wake-up signal to be sent to the translator 302c to cause transition instructions to be inserted into the pipeline following the mode switch instructions.

The Trivedi text at column 8, lines 35-58 identifies that the detector 306 can also include logic to predict whether a switch instruction is likely to be committed. This functionality is performed apparently and mainly to determine whether the detector should or should not signal the speculative wake-up signal to the translator 302c (see Trivedi column 8, lines 44-46). It should be clear, in view of the above, that detector 306 (which the Examiner appears to be equating with the "prediction logic" of claim 1) does not predict when instructions should be prefetched by the prefetch unit and does not indicate to the prefetch unit an address from which a next instruction should be received.

Additionally, the last paragraph in Applicants' independent claim 1 indicates that an instruction set identification signal is generated for sending "to the processor to indicate the instruction set to which said next instruction belongs." The Examiner has identified nothing in the Trivedi reference which suggests this aspect of Applicants' "prediction logic." Given that the existence of a processor core in Applicants' independent claim 1 and in the Trivedi reference is the only common structure between claim 1 and the Trivedi patent, there is simply no support establishing a *prima facie* basis of unpatentability of claim 1 over the Trivedi reference and any further rejection thereunder is respectfully traversed.

Inasmuch as claim 1 is not rendered obvious by Trivedi, claims 2-12 dependent thereon cannot be rendered obvious by Trivedi. Independent claims 13 and 14 incorporate similar limitations as discussed in claim 1, and therefore the above arguments distinguishing claim 1

from Trivedi are herein incorporated by reference in distinguishing claims 13 and 14 from the Trivedi reference.

In view of the above, the Examiner has simply failed to provide any *prima facie* basis for alleging that Trivedi renders obvious the subject matter of Applicants' independent claims and any further rejection thereunder is respectfully traversed.

The Examiner's indication that claims 4-7 and 9-11 contain allowable subject matter and would be allowed if rewritten in independent form is very much appreciated. However, in view of the apparent allowability of claim 1, it is believed unnecessary to rewrite claims 4-7 and 9-11 in independent form. However, the notice of allowable subject matter is very much appreciated.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 1-14 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact Applicants' undersigned representative.

Respectfully submitted,

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